

**Amendments to the Claims:**

Please amend claims 1-3, 5-6, 8-11 and 17 and cancel claim 4 as indicated below. This listing of claims will replace all prior versions and listing of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A circuit for generating a reference current, comprising:  
  
a positive feedback loop coupled with a floating current mirror; and  
  
a negative feedback loop diverting current from the floating current mirror,  
  
wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages.
2. (Currently Amended) The circuit of claim 1, where the negative feedback loop diverts current directly from the floating current mirror.
3. (Currently Amended) The circuit of claim 1, where the negative feedback loop diverts current from the floating current mirror by using a voltage follower.
4. (Canceled)
5. (Currently Amended) The circuit of claim 1, wherein the floating current mirror includes a pair of p-channel transistors.
6. (Currently Amended) A method for providing a current reference, comprising:  
  
providing a current mirror circuit portion;  
  
providing a positive feedback loop portion coupled with the current mirror circuit portion;  
[[and]]  
  
providing a negative feedback loop portion diverting current from the floating current mirror circuit portion; and  
  
operating the current reference with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages.

7. (Original) The method of claim 6, wherein the operation of providing the current mirror circuit portion includes providing a pair of p-channel transistors.
8. (Currently Amended) The method of claim 6, wherein operation of providing the negative feedback loop portion includes diverting current directly from the floating current mirror circuit portion.
9. (Currently Amended) The method of claim 6, wherein the operation of providing the negative feedback loop portion includes providing a control of a common voltage of the current mirror circuit portion.
10. (Currently Amended) A circuit providing a current reference, comprising:
  - a floating current mirror including a first transistor and a second transistor;
  - at least one resistor defining a voltage node;
  - a pull-down transistor; and
  - an output transistor;

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto;

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor; and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor.
11. (Currently Amended) The circuit of claim 10, wherein the pull-down transistor has one end coupled with the floating current mirror and a gate coupled with the voltage node, so as the amount of current provided by the first transistor increases, the pull-down transistor diverts an amount of current received by the first transistor.
12. (Original) The circuit of claim 10, wherein the first and second transistors are p-channel MOSFETS.

13. (Original) The circuit of claim 10, wherein the amount of current mirrored to the second transistor provides a bias signal to the output transistor.
14. (Original) The circuit of claim 10, wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages.
15. (Original) The circuit of claim 10, wherein the pull-down transistor is an n-channel MOSFET.
16. (Original) The circuit of claim 10, wherein the output transistor is an n-channel MOSFET.
17. (Currently Amended) The circuit of claim 10, further comprising:  
  
a protection transistor coupled between the pull-down transistor and the floating current mirror.
18. (Original) The circuit of claim 17, wherein the protection transistor is a p-channel MOSFET.
19. (Original) The circuit of claim 10, wherein a load is coupled to the output transistor, the load receiving the current reference.